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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/075,422	02/13/2002	Michael Brooks	37829.0300/01-0609	7559

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EXAMINER	
ROMAN, ANGEL	
ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 03/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/075,422	Applicant(s) BROOKS, MICHAEL	
	Examiner Angel Roman	Art Unit 2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *9-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election of group I (claims 1-8) in Paper No. 4 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 2 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Takiar et al. U.S. Patent 5,422,435 A.

Takiar et al. discloses a stacked-die semiconductor package comprising; a package substrate 152 having a plurality of bond pads provided thereon, a first

semiconductor device 146 mounted on the package substrate 152, the first semiconductor device 146 having a plurality of bond pads provided thereon, an interposer 148 mounted on the first semiconductor device 146, the interposer 148 having a first interposer bond pad and a second interposer bond pad, wherein the first and second interposer bond pads are electrically coupled to a second semiconductor device 150 mounted on the interposer 148, the second semiconductor device 150 having a plurality of bond pads provided thereon, a first bond wire connected to one of the plurality of bond pads on the first semiconductor device 146 and to the first interposer bond pad; and a second bond wire connected to the second interposer bond pad and to one of the plurality of bond pads on the second semiconductor device 150 (see figures 5 and 6). The semiconductor package further comprising a third bond wire connected to one of the plurality of bond pads on the package substrate 152 and to one of the plurality of bond pads on the first semiconductor device 146.

4. Claims 1, 2 and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Haba et al. U.S. Patent 6,376,904 B1.

Haba et al. discloses a stacked die package comprising; a package substrate 420 having a top side and a bottom side, the top side having a plurality of bond pads provided thereon, and the bottom side having a ball-grid array pattern provided thereon, a first semiconductor device 410a mounted on the top side of the package substrate 420, the first semiconductor device 410a having a plurality of bond pads provided thereon; a silicon interposer 410b mounted on the first semiconductor device 410a, the

interposer 410b having a first interposer bond pad and a second interposer bond pad, wherein the first and second interposer bond pads are electrically coupled via a conductive trace (see figure 11), and wherein the interposer 410b includes an interposer substrate 1002, a dielectric layer 1104 formed on the interposer substrate 1002; a conductive trace 1012 formed on the dielectric layer 1104; and a second semiconductor device 410c mounted on the interposer 410b, the second semiconductor device 410c having a plurality of bond pads provided thereon, a first bond wire connected to one of the plurality of bond pads on said first semiconductor and to the first interposer bond pad; a second bond wire connected to the second interposer bond pad and to one of the plurality of bond pads on the semiconductor device; and a third bond wire connected to one of the plurality of bond pads on the top side of the package substrate and to a bond pad on the first semiconductor device (see figure 3A).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3, 4 and 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takiar et al. U.S. Patent 5,422,435 A in view of Akagawa U.S. Patent 5,677,576 A.

Takiar et al. is applied as above but lacks anticipation on explaining a connection arrangement for the interposer substrate wherein a dielectric layer is formed on the

interposer substrate; a conductive trace formed on the dielectric layer; and a passivation layer formed on the conductive trace, said passivation layer having first and second windows formed therein to expose the conductive trace in areas defining the first and second bond pads. Akagawa discloses an interposer substrate wherein a dielectric layer is formed on the interposer substrate; a conductive trace formed on the dielectric layer; and a passivation layer formed on the conductive trace, said passivation layer having first and second windows formed therein to expose the conductive trace in areas defining the first and second bond pads (see figure 6). In view of this disclosure, it would have been obvious to a person having ordinary skills in the art at the time the invention was made to use the interposer substrate disclosed in Akagawa in the primary reference of Takiar et al. since Takiar et al. suggest using the disclosed package for different type of substrates (see column 6, lines 51-68). Furthermore, while Takiar et al. does not offer a detailed explanation of the type of substrate interconnection used between the interposer substrate and the semiconductor devices, however a person having ordinary skill in the art at the time the invention was made would have found obvious to describe the interposer substrate used by Takiar et al. as one having a dielectric layer formed on an interposer substrate, a conductive trace formed on the dielectric layer, and a passivation layer formed on the conductive trace, said passivation layer having first and second windows formed therein to expose the conductive trace in areas defining the first and second bond pads since these are conventional features of the type of pad interconnection disclosed in Takiar et al. (see figure 6).

7. Claims 3, 4 and 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haba et al. U.S. Patent 6,376,904 B1in view of Akagawa U.S. Patent 5,677,576 A.

Haba et al. is applied as above but lacks anticipation on using a passivation layer formed on the conductive traces. Akagawa discloses a passivation layer 42 formed on conductive traces. In view of this disclosure, it would have been obvious to a person having ordinary skills in the art at the time the invention was made to form a passivation layer on the conductive traces in the primary reference of Haba et al. as disclose in Akagawa et al. since it would prevent contamination and short circuit of the interconnections and it would also protect the conductive traces.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ozawa, Khandros et al., Eichelberger et al., Sawatani and Ishikura disclose stacked-die semiconductor packages comprising at least two semiconductor devices disposed on a substrate with an interposer therebetween.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel Roman whose telephone number is (703) 306-0207. The examiner can normally be reached on Monday-Friday 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers

for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

AR
March 20, 2003

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800